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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,270	02/20/2004	Mark Bilak	FIS920040015US1 2269	
32074	7590 08/21/2006		EXAMINER	
INTERNATIONAL BUSINESS MACHINES CORPORATION DEPT. 18G BLDG. 300-482 2070 ROUTE 52 HOPEWELL JUNCTION, NY 12533			CONNOLLY, MARK A	
			ART UNIT	PAPER NUMBER
			2115	
			DATE MAILED: 08/21/2006	

Please find below and/or attached an Office communication concerning this application or proceeding.

		Application No.	Applicant(s)			
Office Action Summary		10/708,270	BILAK, MARK			
		Examiner	Art Unit			
		Mark Connolly	2115			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply						
WHIC - Exter after - If NO - Failu Any	ORTENED STATUTORY PERIOD FOR REPLY CHEVER IS LONGER, FROM THE MAILING DATE assons of time may be available under the provisions of 37 CFR 1.15 SIX (6) MONTHS from the mailing date of this communication. It period for reply is specified above, the maximum statutory period were to reply within the set or extended period for reply will, by statute reply received by the Office later than three months after the mailing and patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be timusely and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	N. nely filed the mailing date of this communication, D (35 U.S.C. § 133).			
Status						
2a)	Responsive to communication(s) filed on <u>15 Air</u> This action is FINAL . 2b) This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Disposition of Claims						
5)□ 6)⊠ 7)□	Claim(s) 1-25 is/are pending in the application. 4a) Of the above claim(s) 17-24 is/are withdraw Claim(s) is/are allowed. Claim(s) 1-16 and 25 is/are rejected. Claim(s) is/are objected to. Claim(s) are subject to restriction and/o	vn from consideration.				
Applicati	on Papers					
10)	The specification is objected to by the Examine The drawing(s) filed on is/are: a) acception acception and acception and acception acception and acception acception and acception acceptance acception acceptance acception acceptance	epted or b) objected to by the I drawing(s) be held in abeyance. Sec ion is required if the drawing(s) is ob	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).			
Priority u	ınder 35 U.S.C. § 119					
a)(Acknowledgment is made of a claim for foreign All b) Some * c) None of: 1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureausee the attached detailed Office action for a list	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	on Noed in this National Stage			
Attachmen	t(s)					
2) Notic 3) Inform	e of References Cited (PTO-892) e of Draftsperson's Patent Drawing Review (PTO-948) mation Disclosure Statement(s) (PTO-1449 or PTO/SB/08) r No(s)/Mail Date <u>2/20/04</u> .	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:				

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DETAILED ACTION

1. Claims 1-16 and 25 have been presented for examination.

2. Claims 17-24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim.

Election was made without traverse in the reply filed on 8/15/06.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

- (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
- 4. Claims 1-10, 12, 15-16 and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujioka et al [Fujioka] JP 2001142589 A.
- 5. Referring to claim 1, Fujioka teaches the apparatus for adaptively controlling power consumption within an electronic system comprising:
 - a. an integrated circuit adapted to transmit voltage control information, wherein said voltage control information corresponds to a minimum operating voltage of said integrated circuit [fig. 1 and abstract].
 - b. a storage element coupled to said integrated circuit, adapted to store said voltage control information [fig. 1 and abstract].
 - c. a variable voltage regulator coupled to said integrated circuit, adapted to receive said voltage control information from said integrated circuit, and supply an operating voltage to said integrated circuit in response to said voltage control information [0037].

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d. a communication link coupled to said integrated circuit and said variable voltage regulator, adapted to link said integrated circuit to said variable voltage regulator so that said integrated circuit may transmit said voltage control information to said variable voltage regulator [0048].

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- 6. Referring to claim 2, Fujioka teaches the voltage control information is determined during external testing of the IC [abstract].
- 7. Referring to claim 3, Fujioka teaches the storage element being a non-volatile memory [0073].
- 8. Referring to claim 4, Fujioka teaches a temperature sensor for measuring the temperature of the integrated circuit [0037].
- 9. Referring to claim 5, Fujioka teaches modifying voltage control information in response to temperature data [0011].
- 10. Referring to claim 6, Fujioka teaches a built-in-self-test [abstract and 0055].
- 11. Referring to claim 7, Fujioka teaches a temperature sensor for measuring the temperature of the integrated circuit [0037].
- 12. Referring to claim 8, Fujioka teaches modifying voltage control information in response to temperature data [0011].
- 13. Referring to claims 9-10 and 12, these are rejected on the same basis as set forth hereinabove. Fujioka teaches the apparatus and therefore teaches the method performed by the apparatus.

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- 14. Referring to claim 13, Fujioka teaches adjusting a voltage to an integrated circuit and testing with the lowered voltage in order to determine an effective minimum voltage to be applied to the integrated circuit [0062-0063].
- 15. Referring to claims 15-16, these are rejected on the same basis as set forth hereinabove. Fujioka teaches the apparatus and therefore teaches the method performed by the apparatus.
- 16. Referring to claim 25, this is rejected on the same basis as set forth hereinabove.

 The inventions are distinct, each from the other because of the following reasons:

Claim Rejections - 35 USC § 103

- 17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 18. Claims 11 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujioka as applied to claims 1-10, 12-13, 15-16 and 25 above, and further in view of DeLuca et al [DeLuca] US Pat No 5086501.
- 19. Referring to claim 11, although Fujioka teaches performing a test to determine a minimum operating voltage, it is not explicitly taught that the voltage is determined by testing timing critical paths of the integrated circuit. In particular, Fujioka does not teach that voltage is determined based on the speed of the integrated circuit. DeLuca teaches determining a minimum operating voltage of an integrated circuit based on a required speed [col. 2 lines 26-31 and col. 3 lines 16-17]. It would have been obvious to one of ordinary skill in the art at the time of the invention to include a means to select an appropriate minimum voltage based on speed because

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DeLuca explicitly teaches that under certain activities, certain speeds are required in order for the integrated circuit to operate normally.

20. Referring to claim 14, this is rejected on the same basis as set forth hereinabove.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Connolly whose telephone number is (571) 272-3666. The examiner can normally be reached on M-F 8AM-5PM (except every first Friday).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on (571) 272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Mark Connolly Examiner Art Unit 2115

mc August 16, 2006